Memory Devices

In Korea now,

Samsung : 2010, 30nm 2Gb DDRS DRAM/DDR3 SRAM
2011, Invest US $12 bil. for 20nm & SysLSI.

Hynix : 2010, 26nm MLC- NAND Flash
2011, 30nm 4Gb DRAM

"At 2020, the demands of computing power & stroage capacity will be 60 times greater than now, due to the needs of smart devices.
10nm-3D NAND Flash will be the solution"

Ki-Nam Kim, President, Institut of Technology Samsung Electronics,
2010 IEDM, San Francisco.

SOI

Conventional MOSFET(2D) ⇨ FinFET(3D)
SOI is the most promising to 3D nano-devices

30 years efforts to SOI materials
Heteroepitaxy : SOS, ELO
Recrystallization : ZMR, SPE
Oxidation : FIPOS, ELTRAN
Bonding : SDB, BESOI
Implantation : SIMOX, → **** Smart-Cut™***

Memory Effects in SOI-FinFET with ONO Buried Insulator

Jong-Hyun Lee, Kyungpook National University, Korea

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Advanced SOI Device with Alter. BOX

Conventional
SOI Wafer Structure

Alternative Buried Insulator
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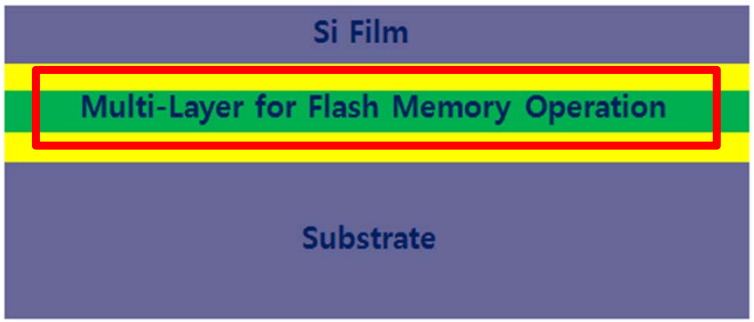
Fin Etch Definition

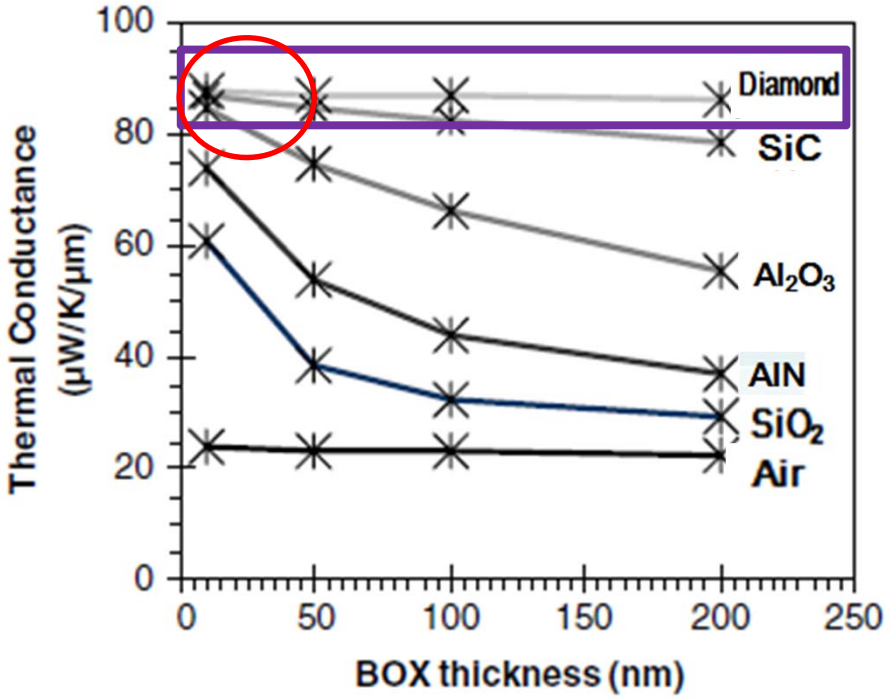


Oxide/Nitride/Oxide Multi Layer
for Flash Memory Application

Applications: Self-Heating Reduction (review)

Material	Thermal Conductivity ($Wm^{-1}k^{-1}$)	Relative Permittivity
Air	2.6×10^{-2}	1
SiO2	1.4	3.9
Diamond	800	5.8
AlN	5	9
Al2O3	20	12
SiC	120	13

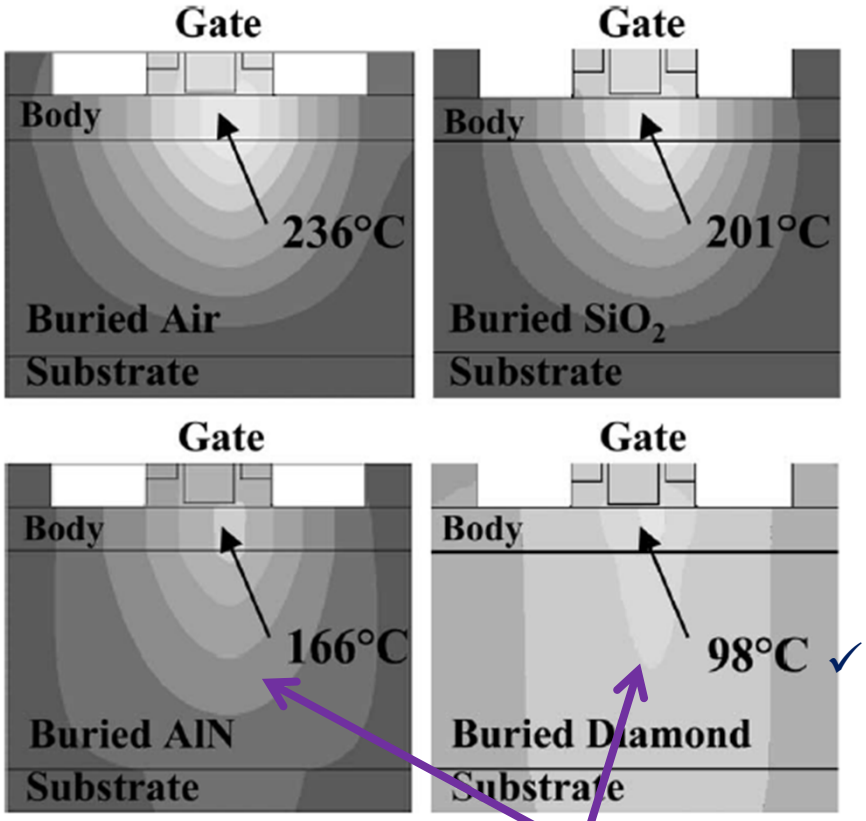
CRC Materials science and engineering handbook

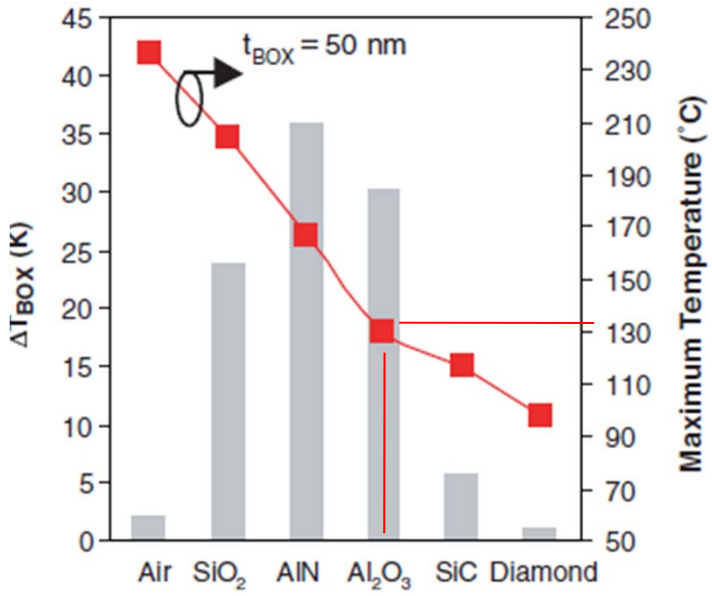


N. Bresson *et al.* / Solid-State Elec. (2005)

✓ Thermal conductance is dominated by the thickness of BOX

Applications: Self-Heating Reduction (review)





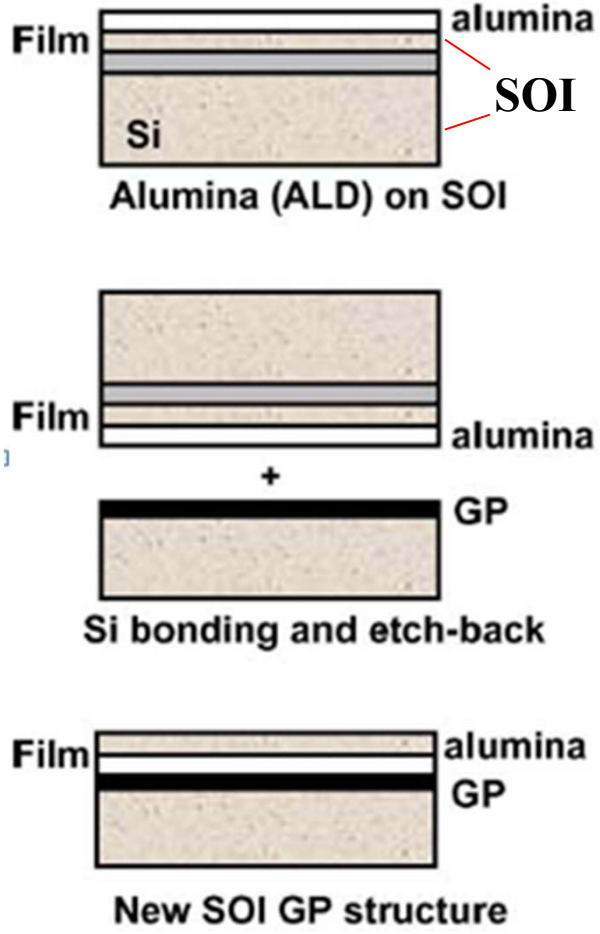
✓ Temperature difference between thick (400nm) and thin (50nm) BOX (columns)

✓ The heat is spreading in the BOX and easily evacuated by the silicon substrate.

✓ Carrier mobility can be improved.

N. Bresson *et al.* / Solid-State Elec. (2005)

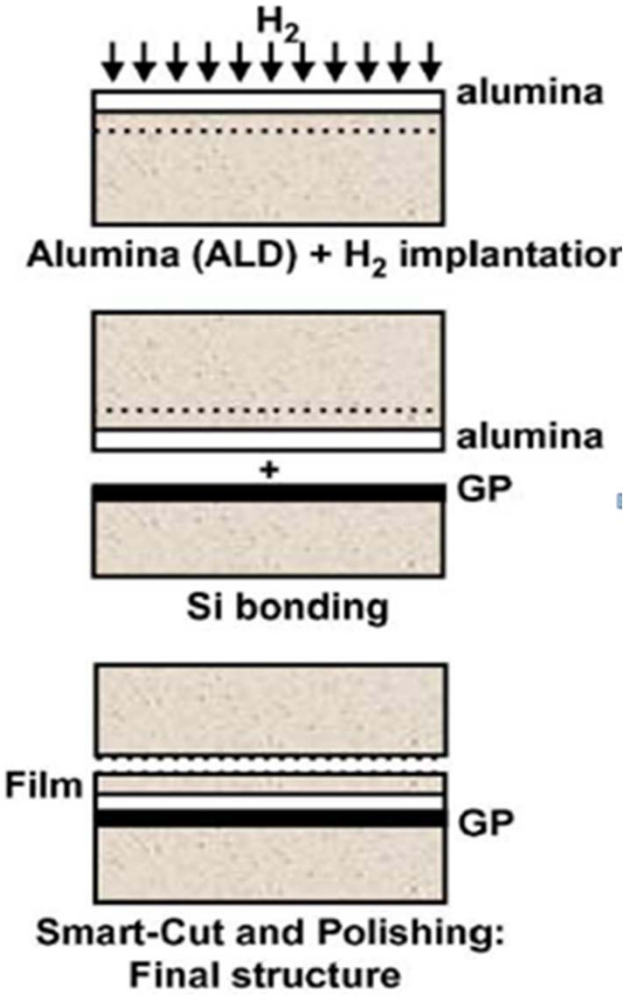
Applications: Short-Channel Effects Reduction (review)



- ✓ Process-flow for SOI wafers with buried alumina and ground-plane
- ✓ Preliminary sequence for the prototype structure
- ✓ GP(ground plane) is p^{+}-Si (10^{19})

K. Oshima et al. / Solid-State Elec. (2004)

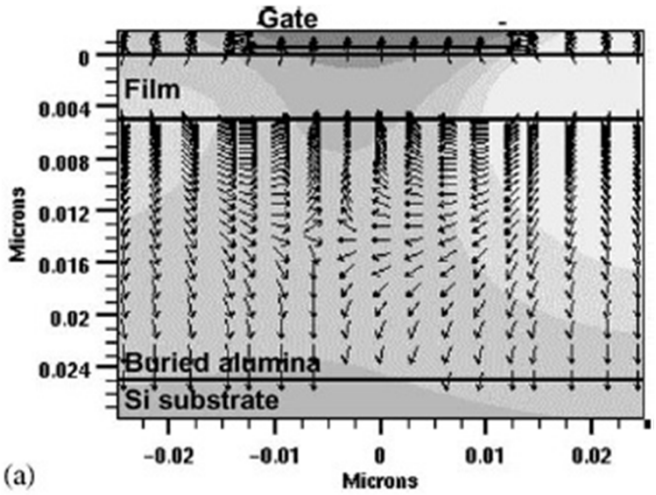
Applications: Short-Channel Effects Reduction (review)

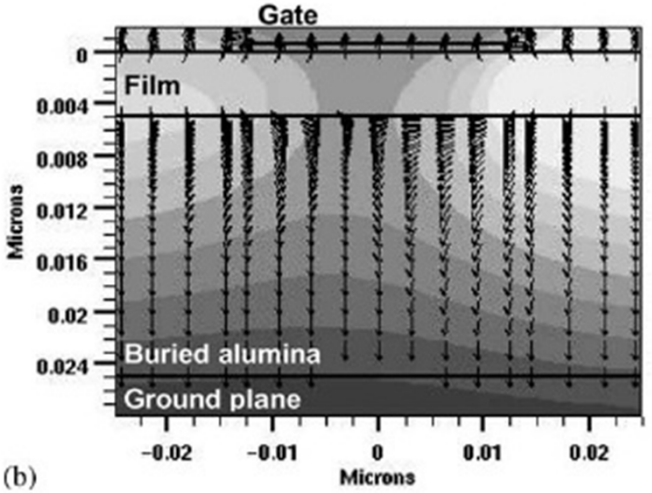


- ✓ Process-flow for SOI wafers with buried alumina and ground-plane
- ✓ Mature process based on Smart-Cut ™.

K. Oshima et al. / Solid-State Elec. (2004)

Applications: Short-Channel Effect Reduction (review)



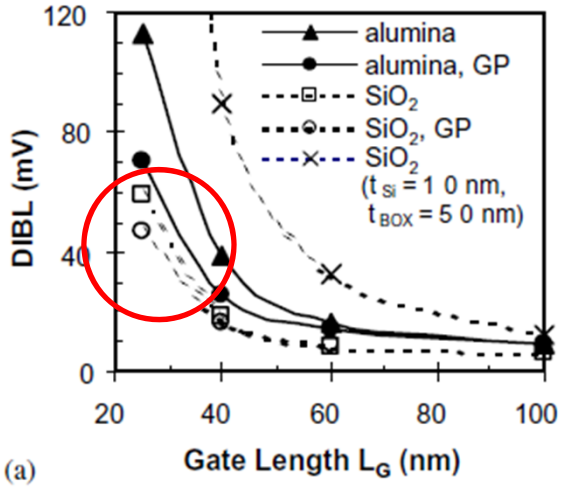


- ✓ Standard configuration:
  the electric field in the top region of the BOX is parallel to the interface

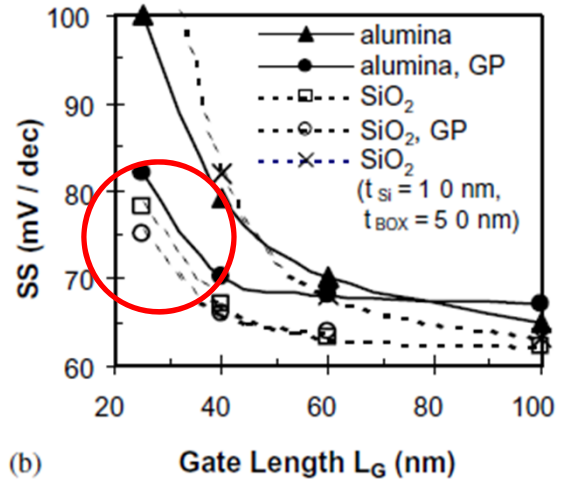
- ✓ Ground Plane:
  near-surface field is turned downward which reduces DIVSB

K. Oshima et al. / Solid-State Elec. (2004)

Applications: Short-Channel Effect Reduction (review)



(a)

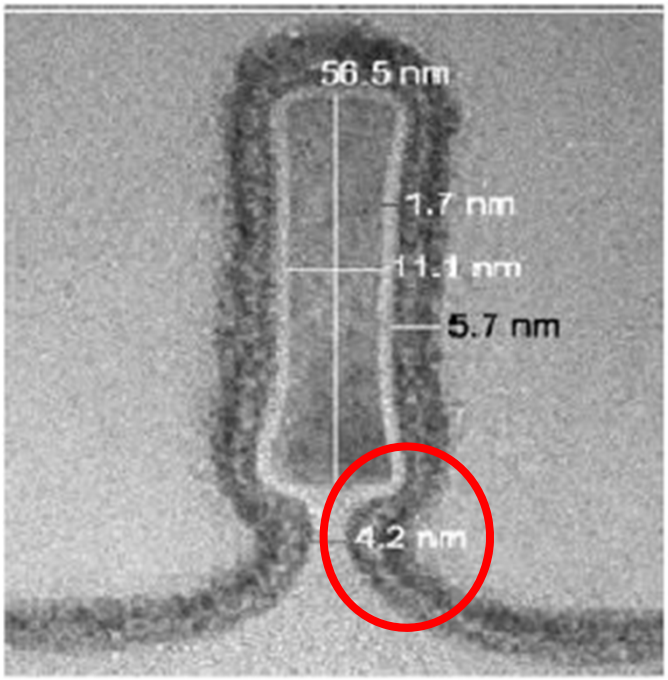


(b)

- ✓ The advantage of the ground plane structure increases for devices shorter than 40 nm.
- ✓ No trade-off between the thermal and electrical characteristics of SOI MOSFETs with buried alumina is necessary, even for extremely short deivce.

K. Oshima et al. / Solid-State Elec. (2004)

Applications: Fin Etch Definition (review)

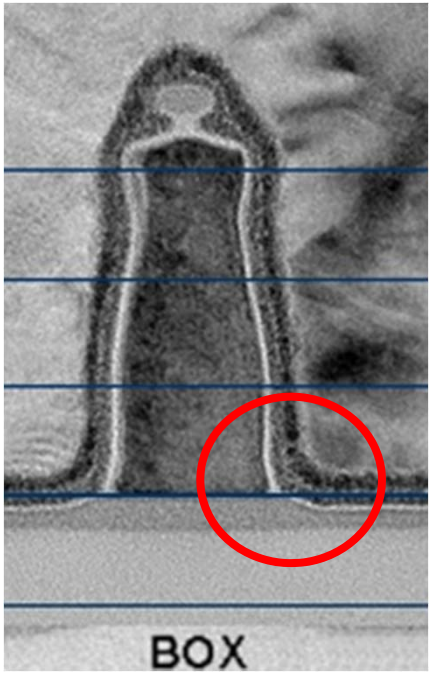


FinFETs with SiO_2 BOX

- ✓ The under-cut in the buried oxide is an inherent by-product of pre-gate clean.
- ✓ Under-cut improves gate control of the channel at fin and BOX interface.
- ✓ Under-cut undermines the fin stability, and increases susceptibility to gate etch defects.
- ✓ During gate etching, the gate material hiding in the under-cut region is difficult to remove and is a source of gate to gate electrical short if not etched completely.

P. Patruno *at al.* / IEEE Inter. SOI Con. Proc. (2007)

Applications: Fin Etch Definition (review)



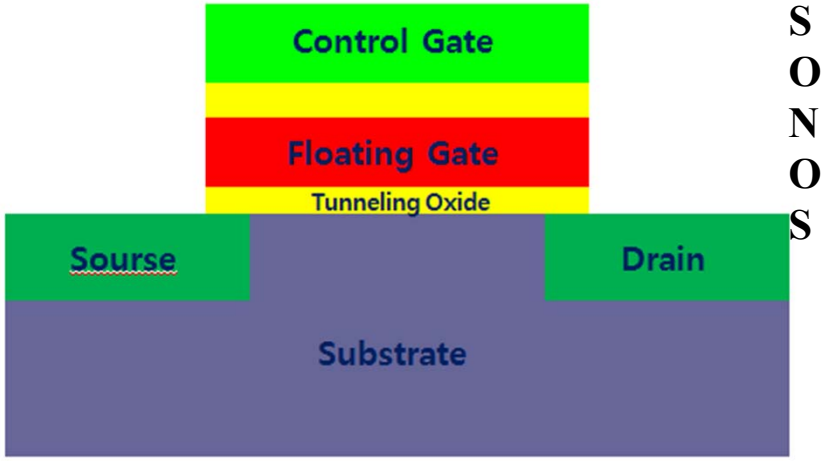
- ✓ The nitride film in the ONO buried layer acts as an etch-stop layer to prevent BOX recess and fin undercut.
- ✓ Maintaining good gate electrode and the static control of the channel at bottom interface

FinFETs with ONO Buried Insulator

P. Patruno *at al.* / IEEE Inter. SOI Con. Proc. (2007)

Flash Memory Concept: Structure (review)

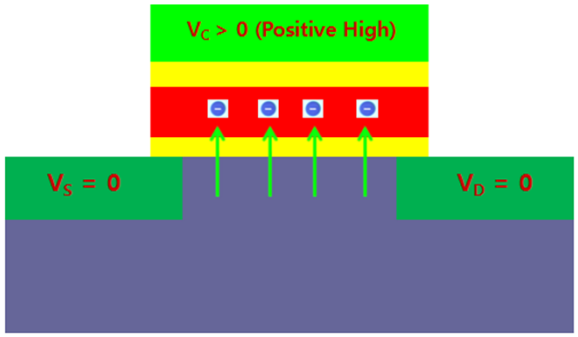
- ✓ Floating Gate Concept: The conventional concept



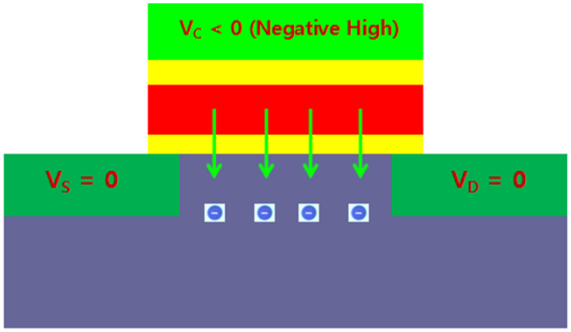
- ✓ The conventional flash memory cells are based on the charge storage in a floating gate which is also used to sense the current.
- ✓ Silicon-oxide-nitride-oxide-silicon (SONOS) structure, where the nitride layer is used to store the charges, has been suggested.
- ✓ SONOS flash memory device is attractive because the SONOS process is simpler and offers good retention characteristics due to the presence of deep trap levels in the nitride.

Flash Memory Concept: Trapping/Detrapping (review)

- ✓ Fowler-Nordhem Tunneling



- ✓ Positive V_C
  - → Electron trapping
  - → Threshold voltage decreases
  - → Low level drain current

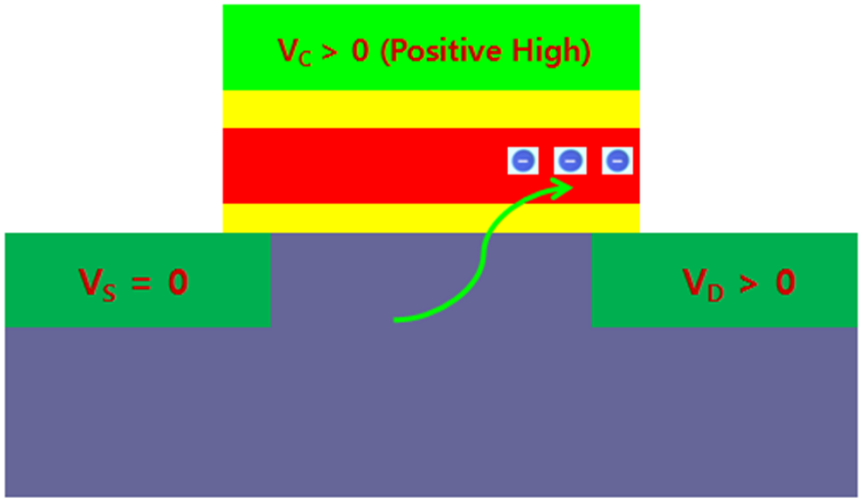


- ✓ Negative V_C
  - → Electron detrapping
  - → Threshold voltage increases
  - → High level drain current

- ✓ Quantum-mechanical tunneling induced by an electric field
- ✓ A large electron tunneling current through a thin oxide without destroying its dielectric properties

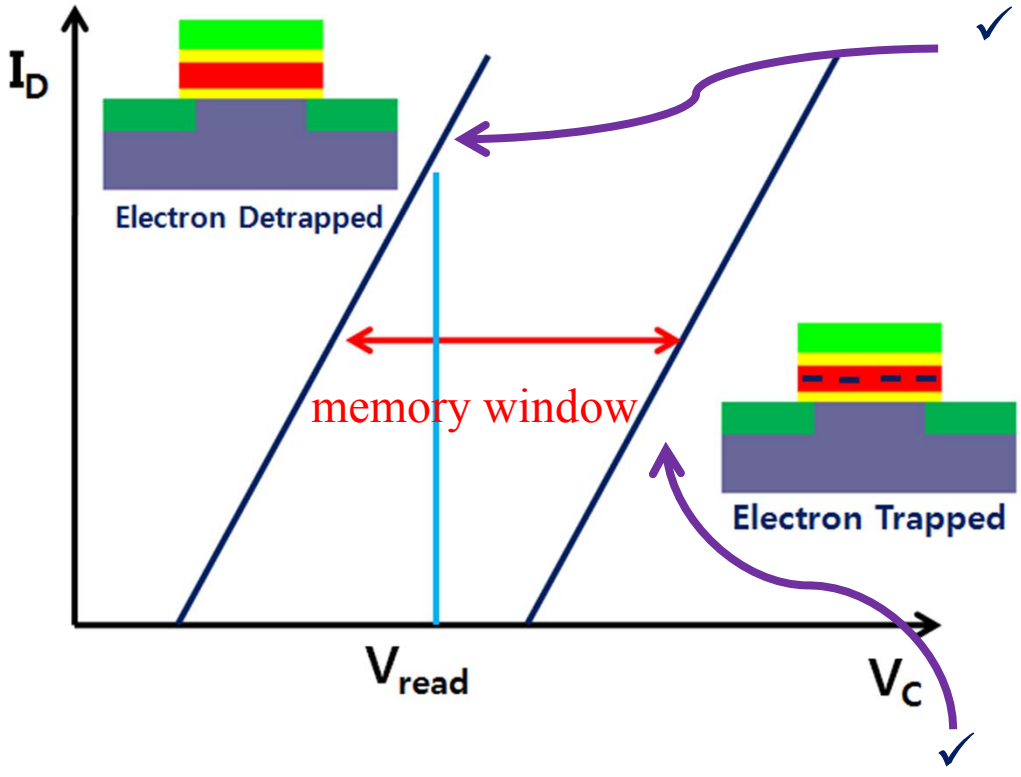
Flash Memory Concept: Trapping/Detrapping (review)

- ✓ Channel Hot Electron



- ✓ The CHE mechanism, where electrons gain enough energy to pass the oxide-silicon energy barrier, thanks to the electric field in the transistor channel between source and drain.
- ✓ Injection in the floating gate at the drain side

Flash Memory Concept: Reading Operation (review)



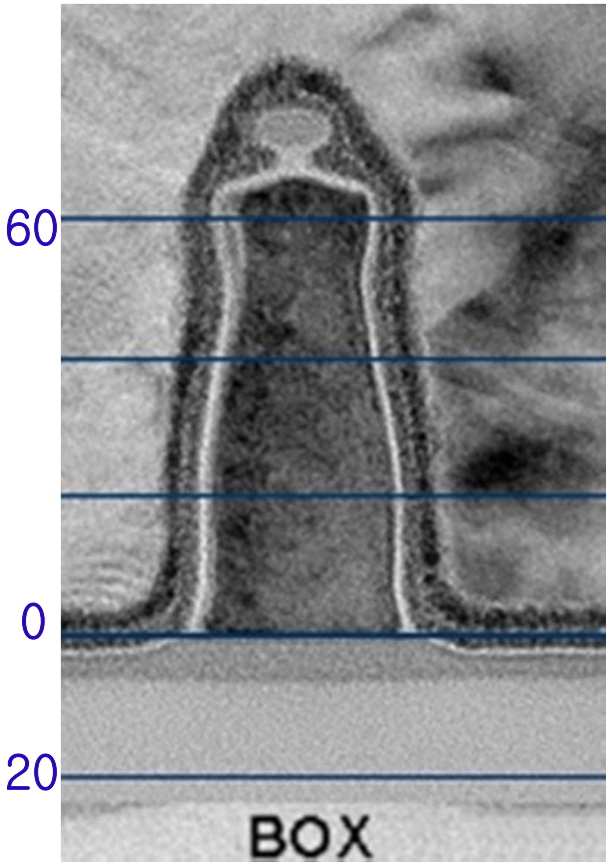
✓ High Current Level:

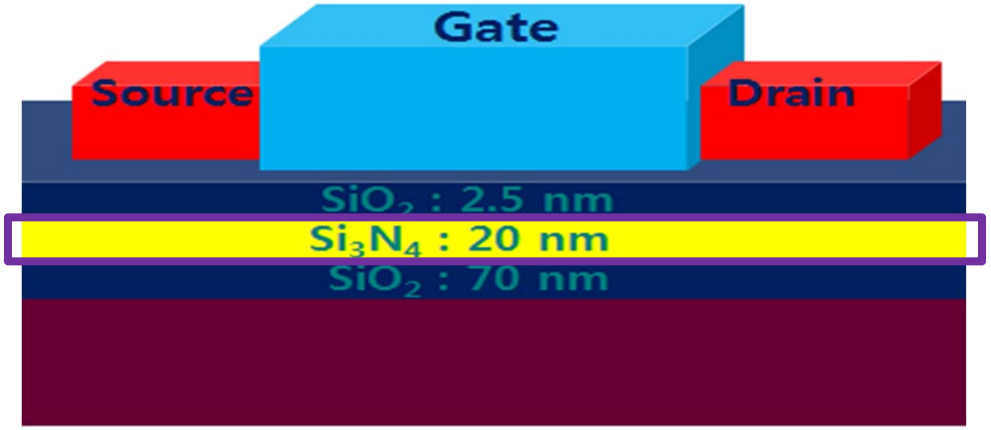
'1' State

✓ Low Current Level:

'0' State

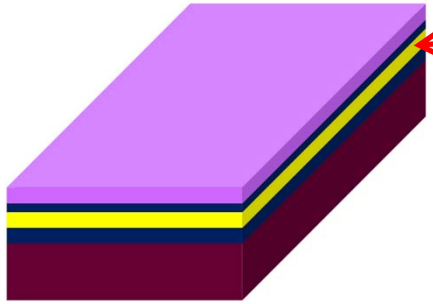
Device Structure (FinFET on ONO)





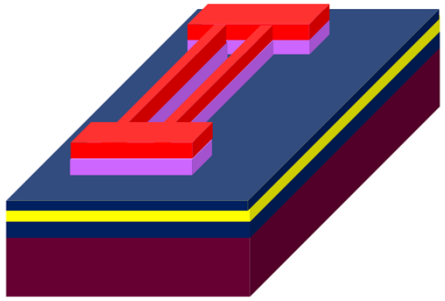
- Alternative Buried Insulator Structure
  → **SiO_2 (2.5 nm) : Si_3N_4 (20 nm) : SiO_2 (70 nm)**
- **Thin SiO_2 (2.5 nm) Buried Layer**
  → **Carrier Tunneling**
- **Si_3N_4 (20 nm) Buried Layer**
  → **Charge Storage for Flash Memory Application**

Device Fabrication Processing

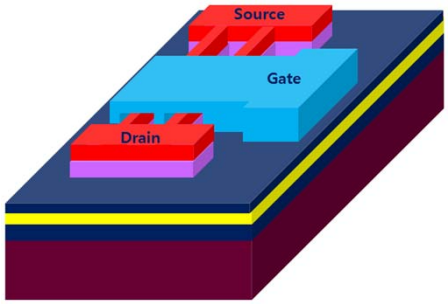


Oxide/Nitride/Oxide Structure

- Starting Material :
  ONO buried insulator

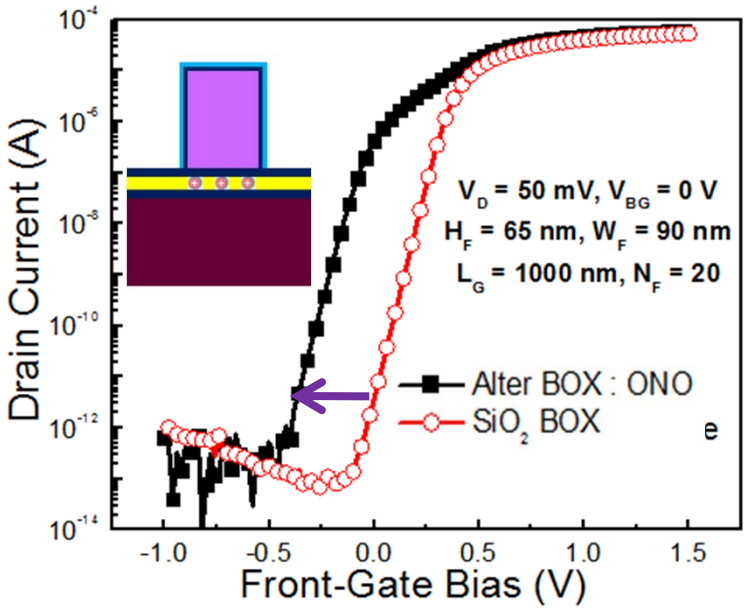


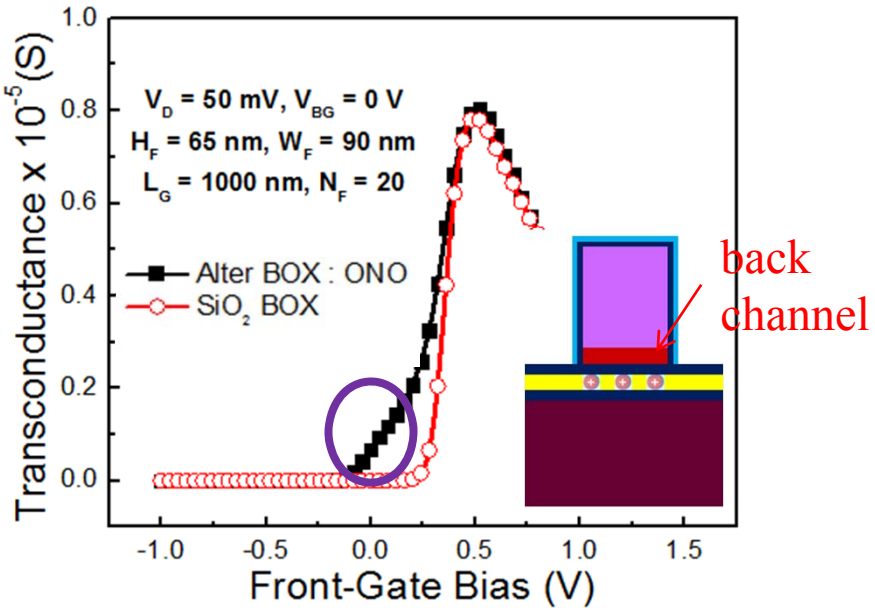
- Si film : 65 nm (Fin Height)
- Gate Oxide : 1.8 nm (Wet Oxidation)
- Hydrogen annealing :
  smooth the fin sidewalls



- Gate Material : TiSiN (LPCVD)

ONO FinFETs Characteristics





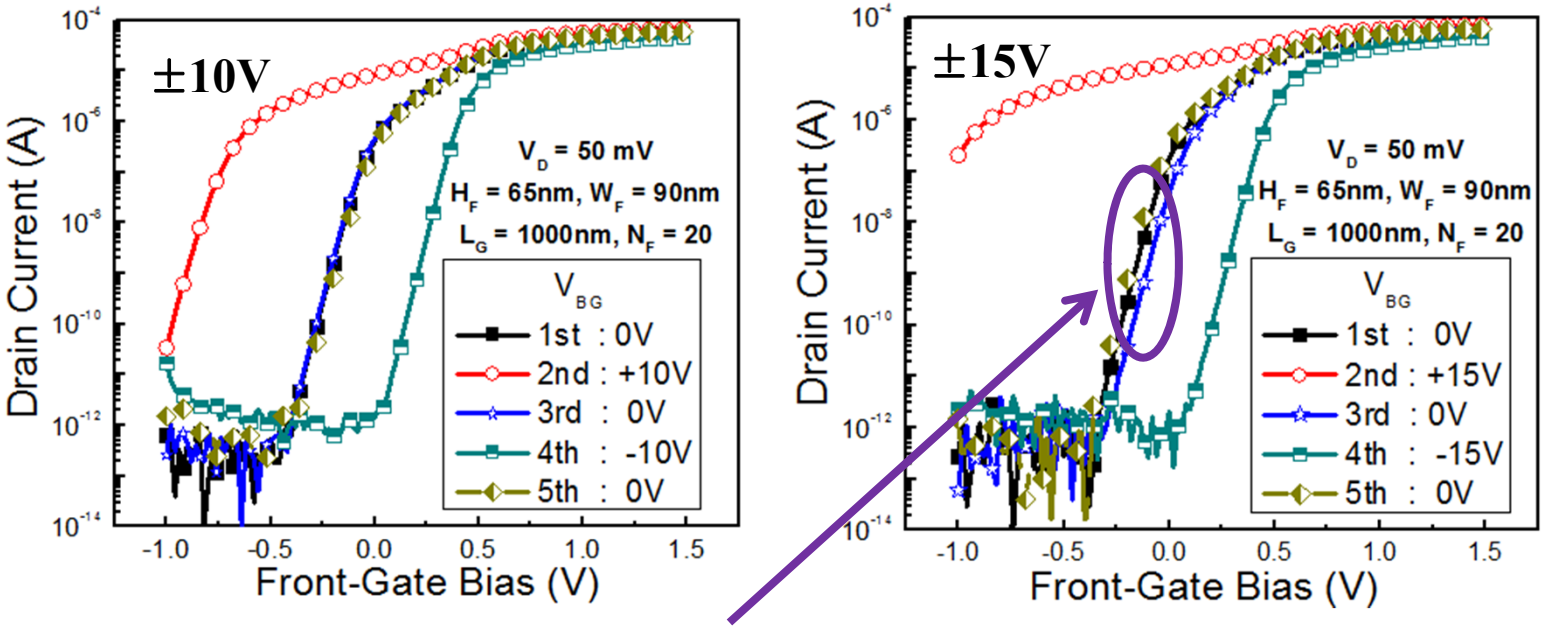
- **Lower Front-Channel Threshold Voltage**

  During fabrication process, positive charges are trapped in Si_3N_4 buried layer → Body potential is increased

- **Hump in the transconductance curve**

  The back channel is easily activated by the positive charges in Si_3N_4 buried layer.

History Effects: by back gate biasing

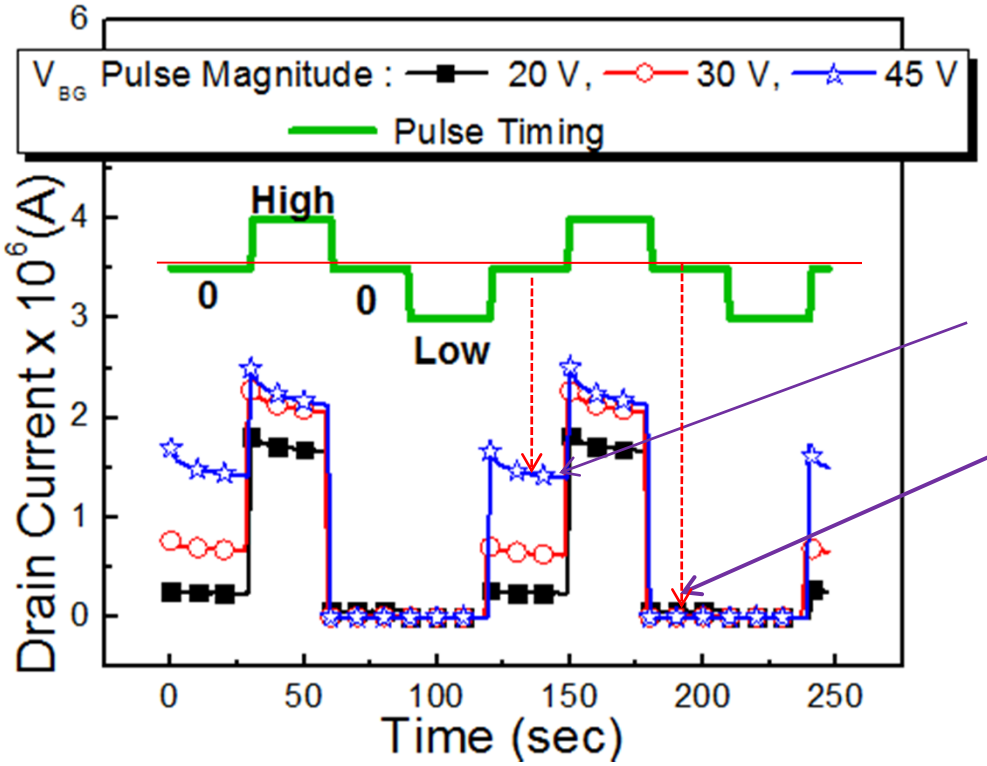


- The curves measured at V_{BG} = 0 V do not overlap.

  Back-gate biasing can lead to charge trapping in the Si_3N_4 buried layer.

- History effects by back-gate biasing occur for V_{BG} > ±15 V.

Transient Effects: by Back-Gate Pulsing



- Transient effect induced by back-gate pulsing.

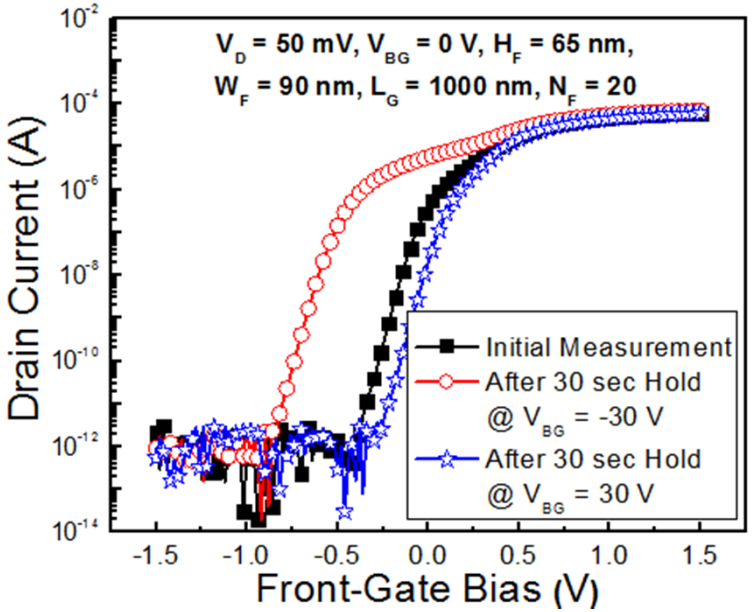
State '1'

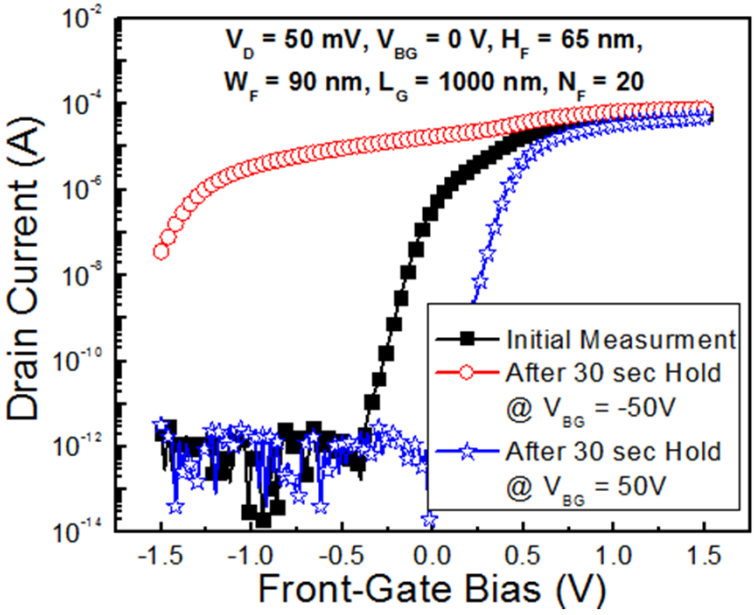
State '0'

- Different drain current level at V_{BG} = 0 V

- Drain current level after switch depends greatly on the voltage before switch.
- This phenomenon is the typical history effects.

Memory Effects





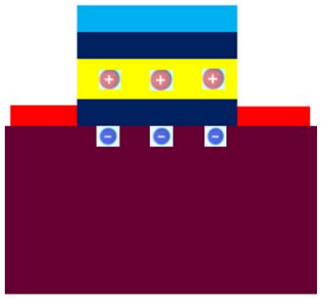
- The charges are trapped from body into Si_3N_4 buried layer through the thin SiO_2 buried insulator.

  ← The charge trapping mechanism is FN Tunneling.

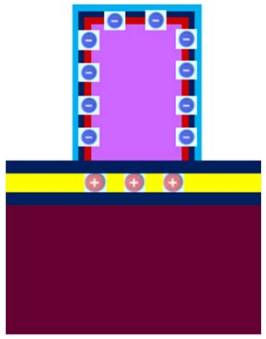
- The shift of $I_D(V_G)$ curve indicates the amount of trapped charges.

  → The amount of trapped charges depends on the back-gate biasing.

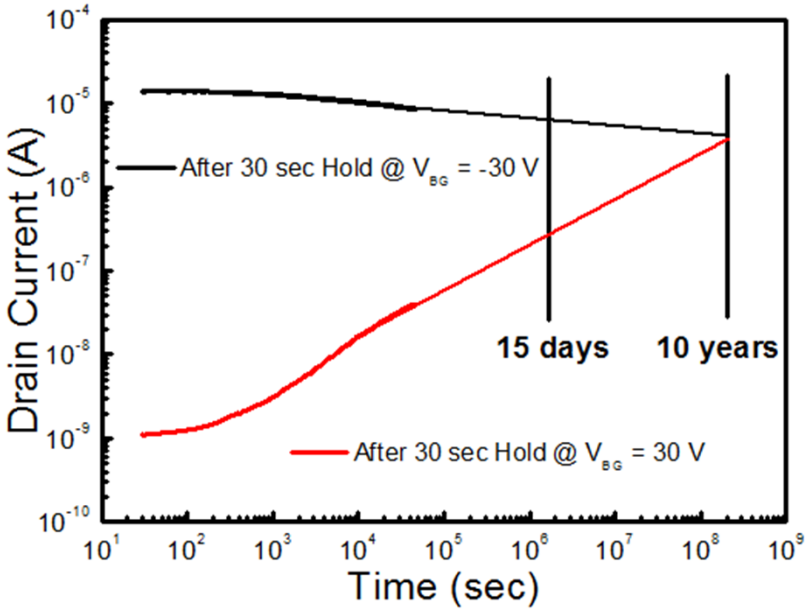
Retention in the Si_3N_4 layer



Conventional



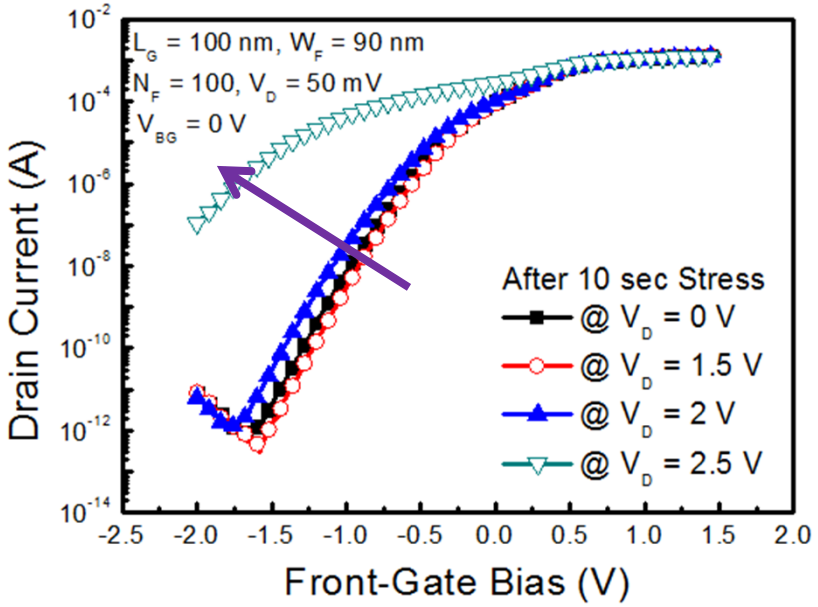
FinFlash
(ONO-SOI)

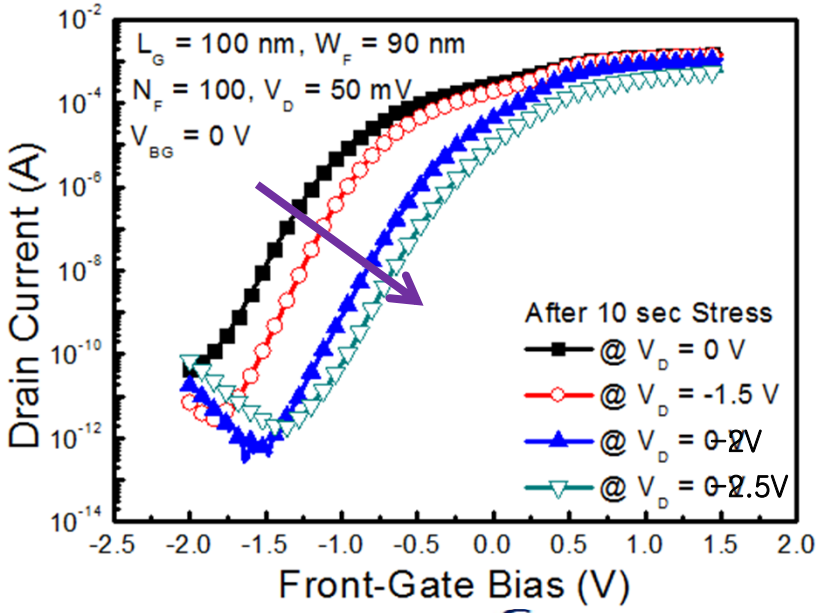


- V_{THF} decreases and back-channel turns on: positive trapped charge.
- The trapped charges are maintained over 15 days.
- **This effect is different from conventional flash cells.**

→ Charges are trapped in the BOX and sensed by the front-channel.

Charge Trapping by High Drain Biasing

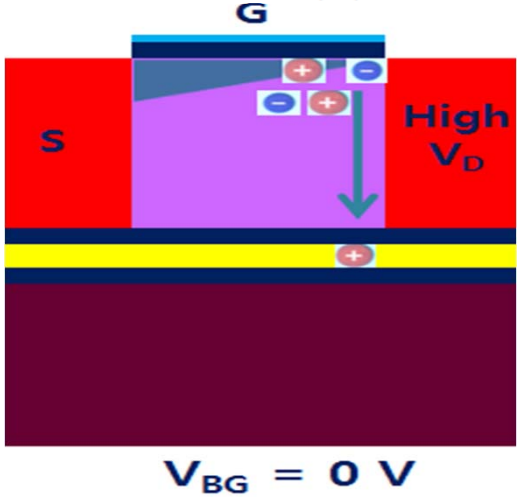




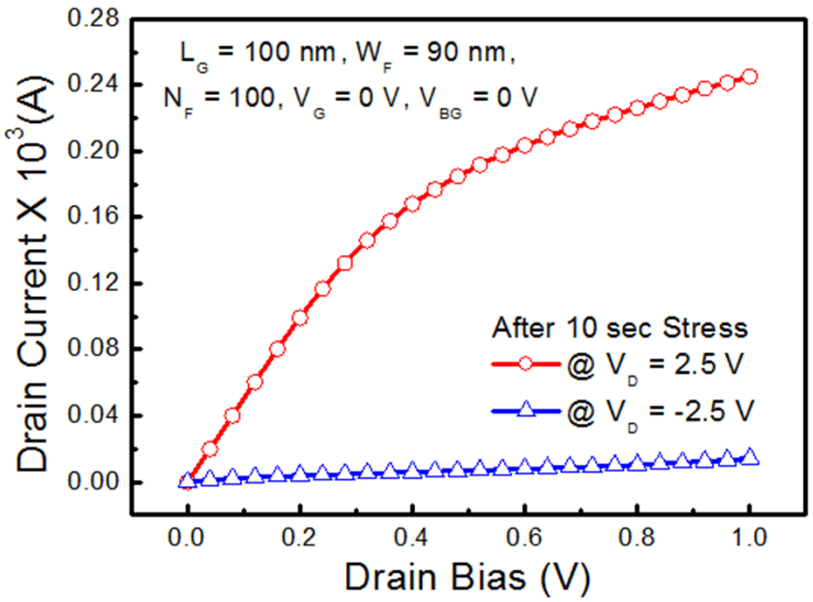
- **High drain biasing can lead to charge trapping in the Si_3N_4 buried layer.**
- Charge Trapping Mechanism

  1st : Impact Ionization by high drain bias

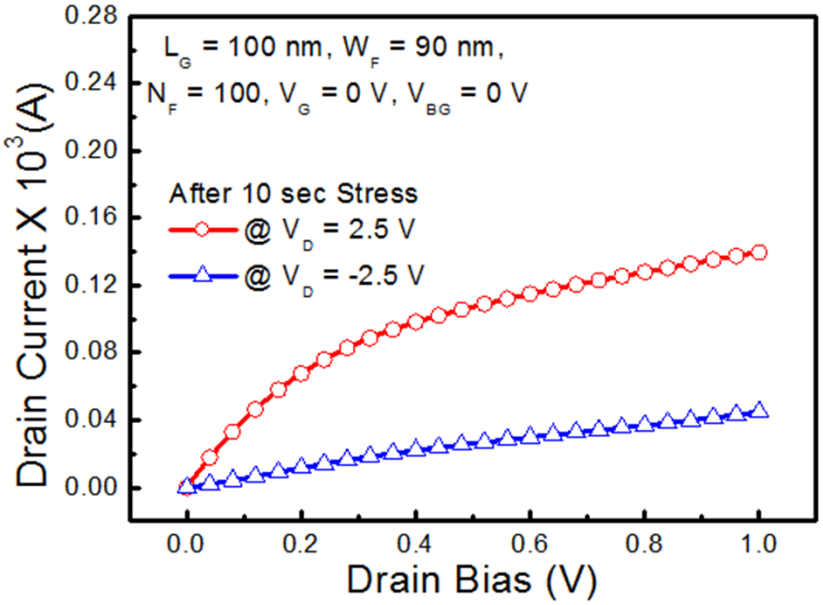
  2nd : Charges are trapped in the Si_3N_4 buried layer by vertical electric field.



Charge Trapping by High Drain Biasing



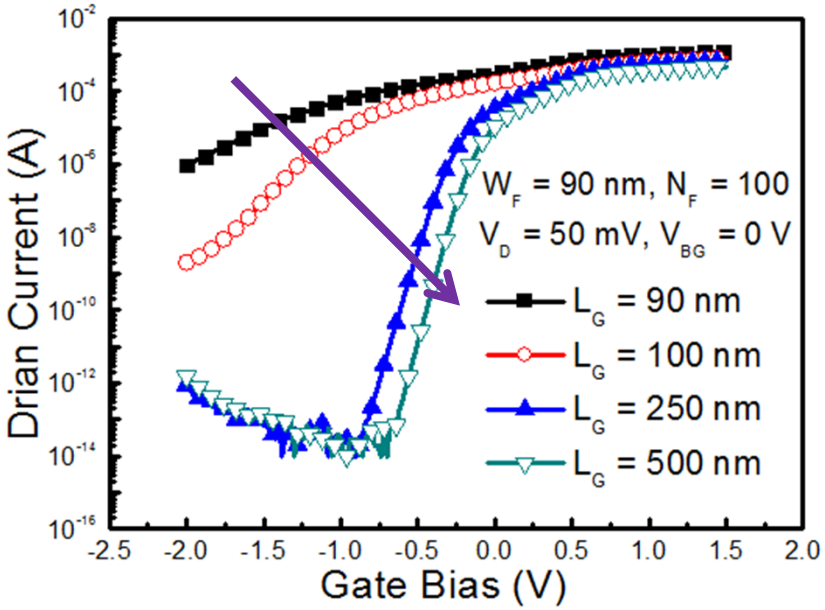
Source-Drain

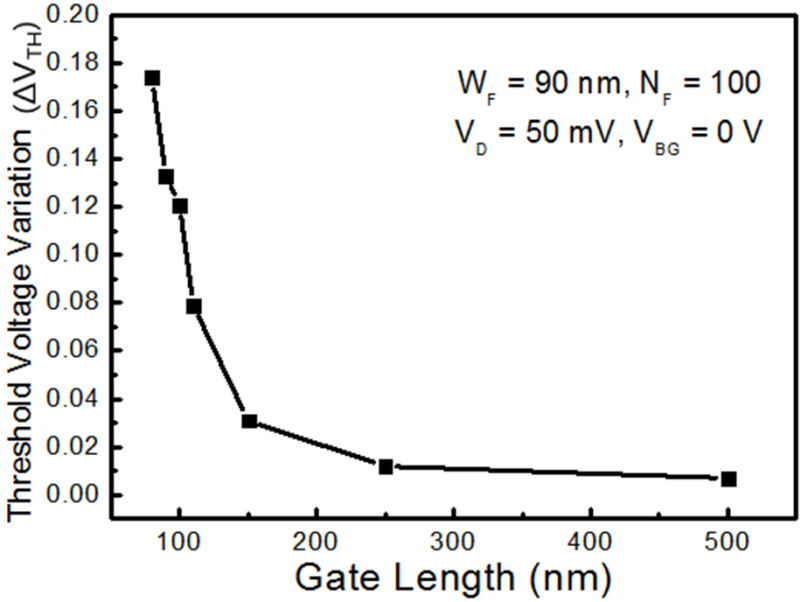


Drain-Source

- ✓ **Positive V_D → remove the trapped electron → high drain current**
- ✓ **The difference in drain current between '0' and '1' is large enough for application in flash memory devices.**
- ✓ **Trapped charges are located near the drain region.**

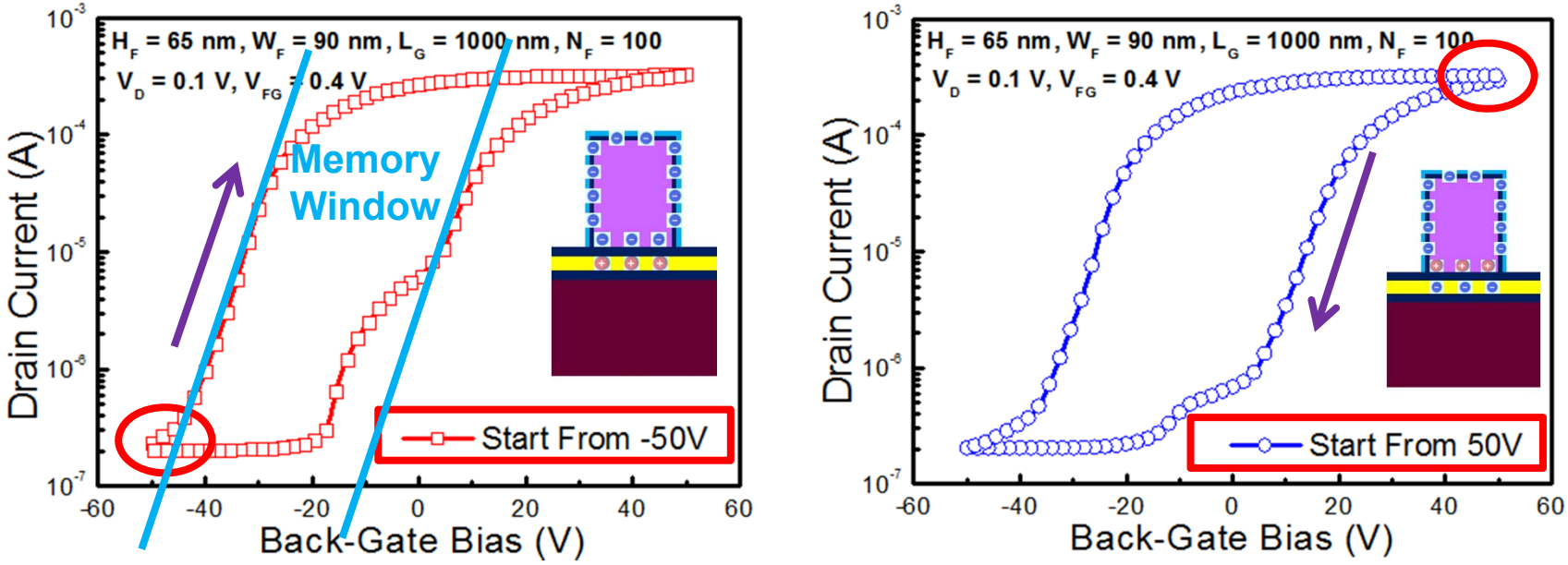
Charge Trapping: gate length dependence





- ✓ The shift in drain current and V_{TH} increases substantially in shorter channel devices.
- ✓ Trapped charges are located near the drain region so that their impact on the current increases in shorter devices.

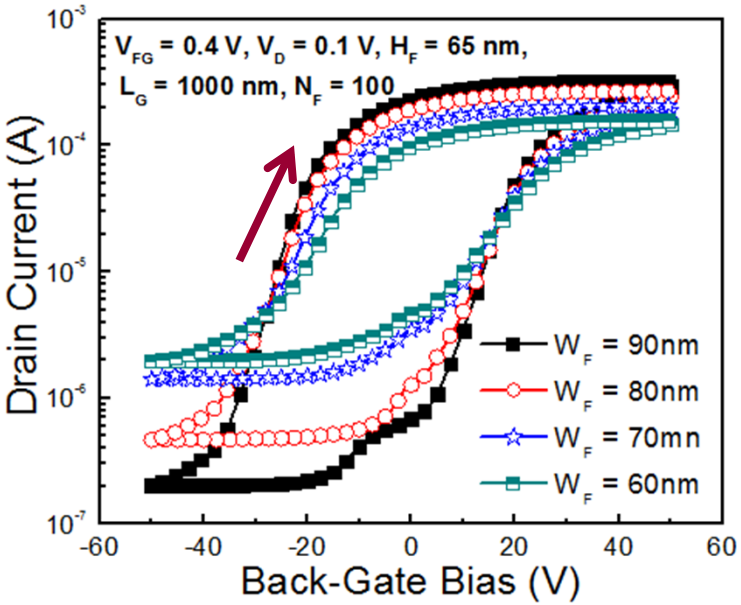
Drain Current Hysteresis

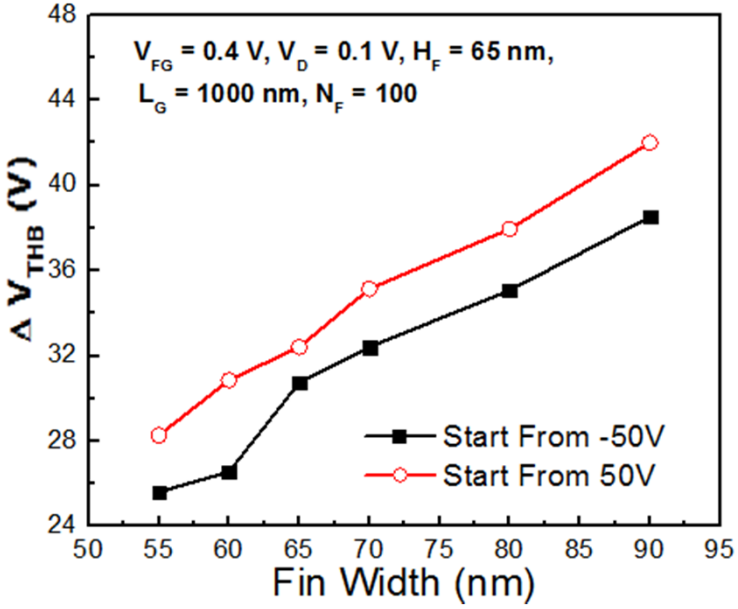


- **Drain current hysteresis, useful as a memory windows, is induced by the shift of V_{TH} due to trapped Si_3N_4.**
- The measurement starting value affects the memory windows size.

  The charge trapping efficiency is different for holes and electrons.

Hysteresis: Fin Width Dependence



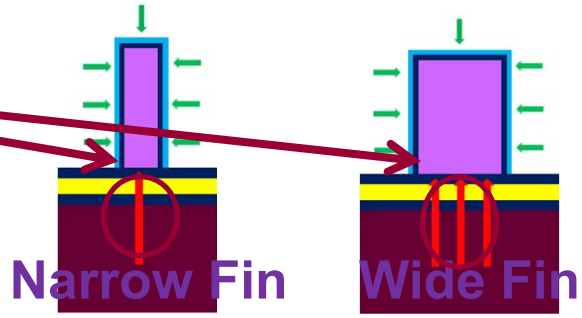


- For wider W_F, the memory window increases.

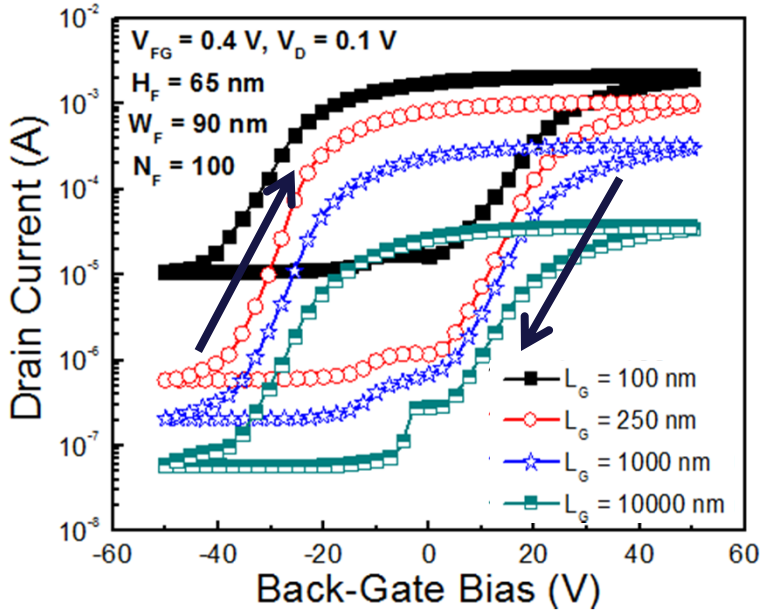
→ **Larger trapping area**

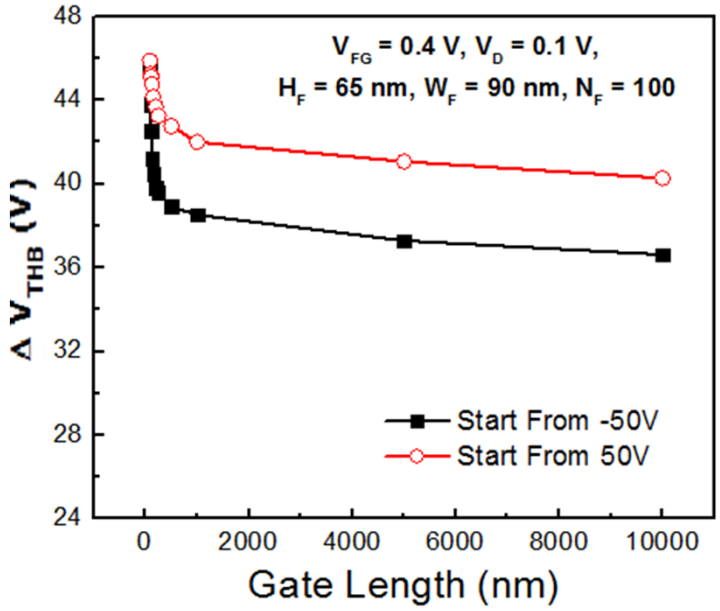
→ **The effect of vertical coupling component increases.**

→ **Gate impact lowered**



Hysteresis: Gate Length Dependence



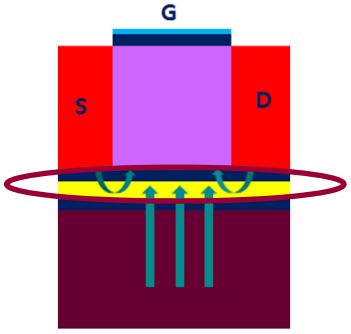


- For shorter L_G, the memory window increases!

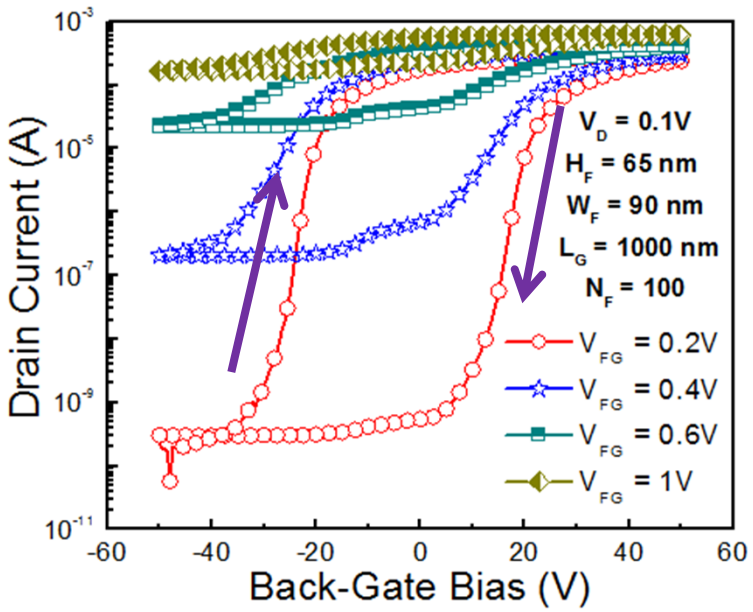
→ For shorter device, the effect of longitudinal coupling component induced by drain bias reinforces the back surface potential.

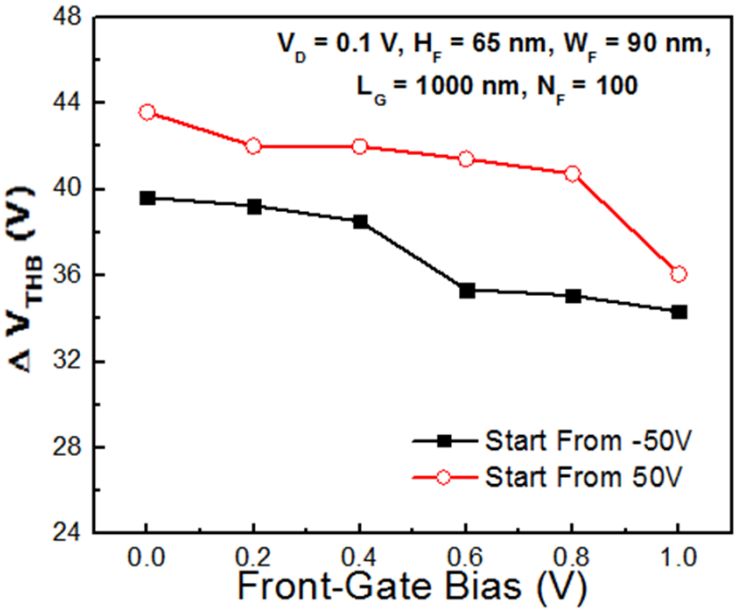
→ Gate effect lowered

→ **Excellent results for scaling**



Hysteresis: Front-Gate Bias Dependence





- For higher V_{FG}, the memory window decreases.

→ The effect of lateral coupling between the lateral gates is increased which tends to block the back surface potential.

→ Trade-off between front and back gate bias

Conclusions

- In ONO buried insulator, Si_3N_4 buried layer can trap charges by back-gate or drain biasing.
- The trapped charges are maintained in the Si_3N_4 buried layer for a long time.
- A large front channel threshold voltage variation, useful for novel memory cell is induced by trapped charge in the Si_3N_4 buried layer.
- The memory window size depends on the bias condition and geometrical parameter.
- The memory window is useful for flash memory and can be combined with 1T-DRAM according to ‘unified’ memory concept.

GaN-MOSFET

GaN is intensively studied for the blue LED last 20 years

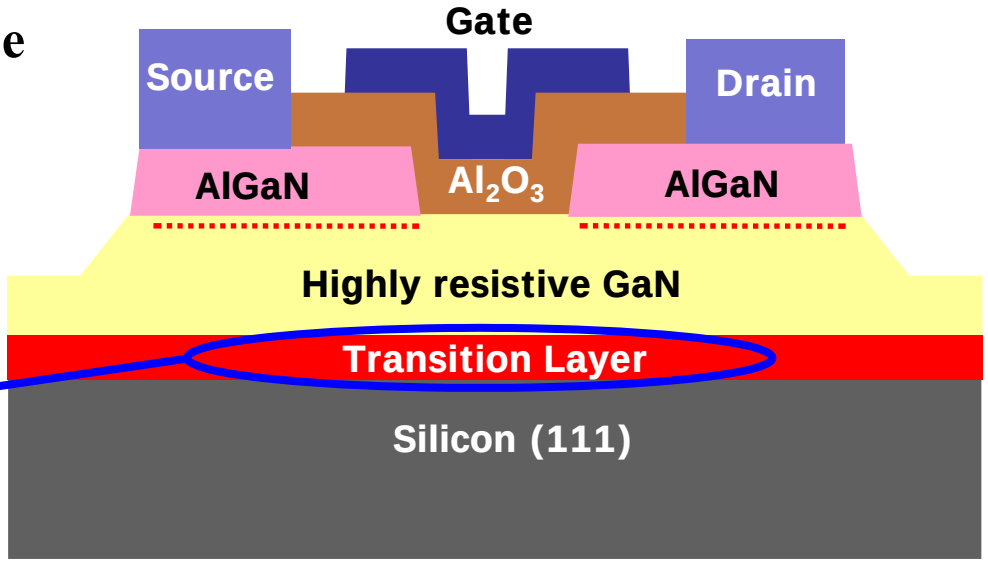
Here, GaN-MOSFET for power device applications

1. Normally-off GaN-MOSFET (high 2DEG density S/D)

➢ **Normally-off GaN MOSFET on Si substrate**

- Fully recessed MIS structure
- Al_2O_3 gate insulator
- Extremely high 2DEG in S/D (>10^{14}/cm^2) : stress controlled
an order higher than normal AlGaN/GaN HFET

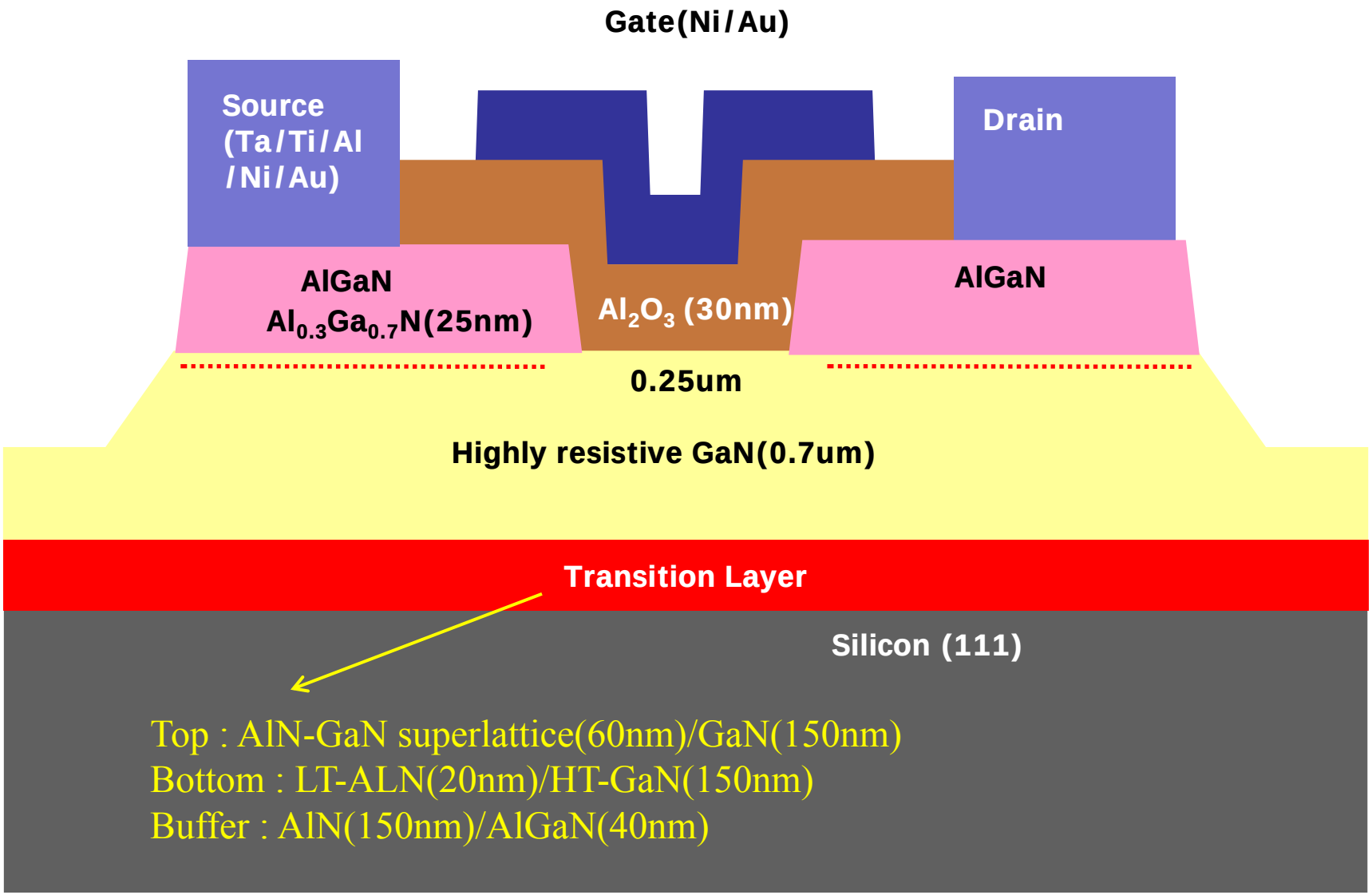
- Supplies many electrons into the channel
- Reduces parasitic series resistance
higher I_D,
higher g_m,
lower R_{on}…..



Transition layer :
Modify stress induced 2DEG density

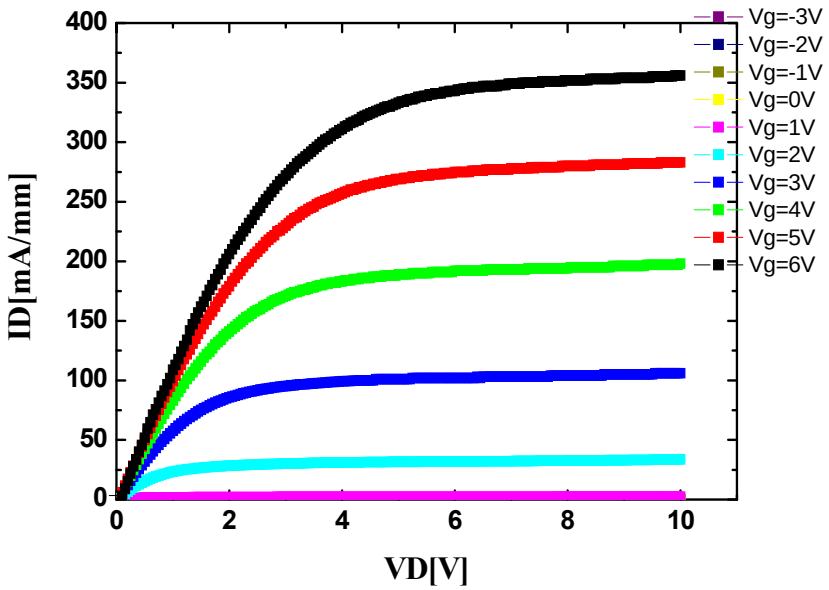
[IEEE Electron Device Letters, Vol.31, No.3, P.192, 2010]

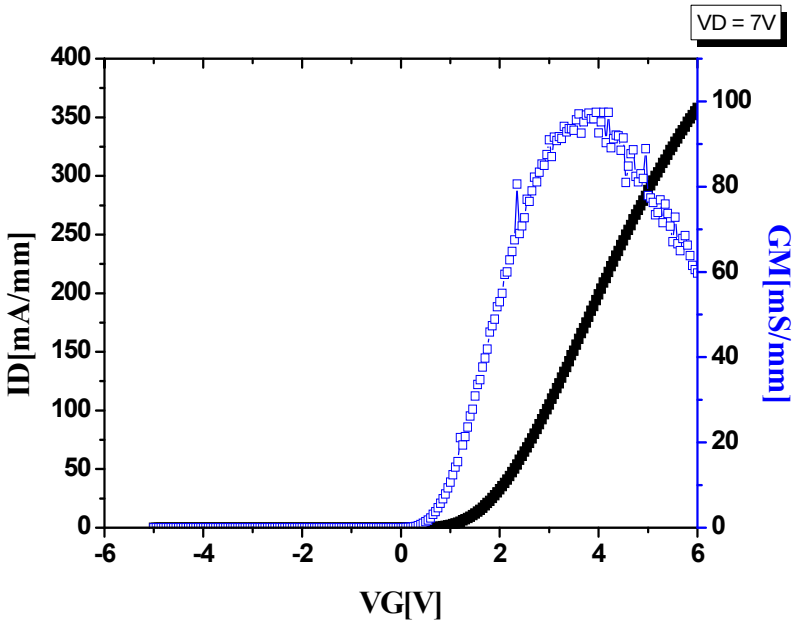
(high 2DEG density S/D)



(high 2DEG density S/D)

[L_g : 0.25 um]



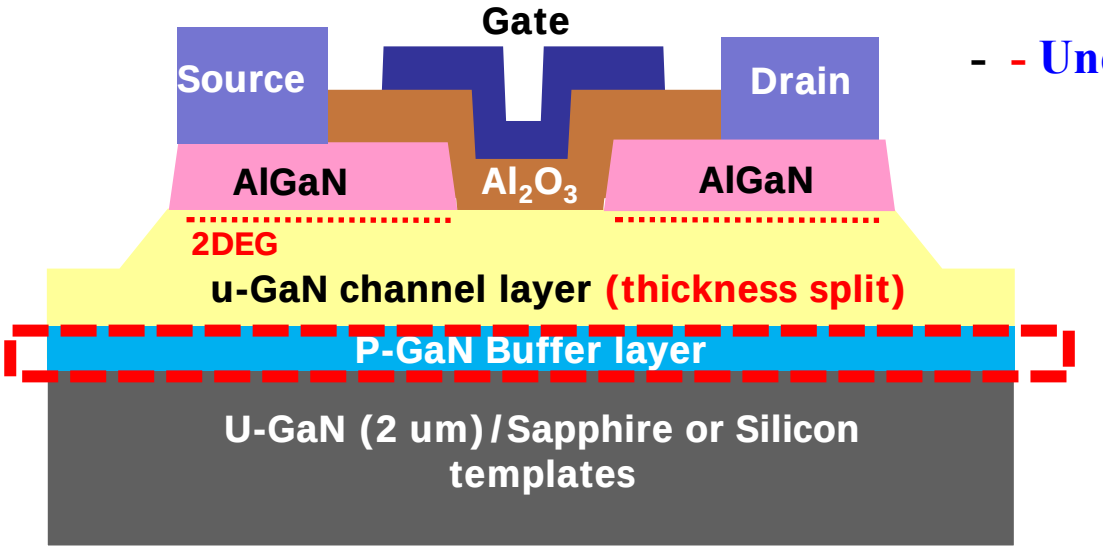


$R_{on}\cdot A = 2.1\ m\Omega\cdot cm^2$,
$I_{d,max} = 353$ mA/mm,
$\mu_{FET} = 225\ cm^2/Vs$,

SS = 317 mV/dec
$g_{m,max} = 98$ mS/mm
$V_{th} = 2.0$ V,

2. Normally-off GaN-MOSFET *(p-GaN back barrier)*

➢ **Control of Threshold Voltage with P-GaN Buffer Layer**

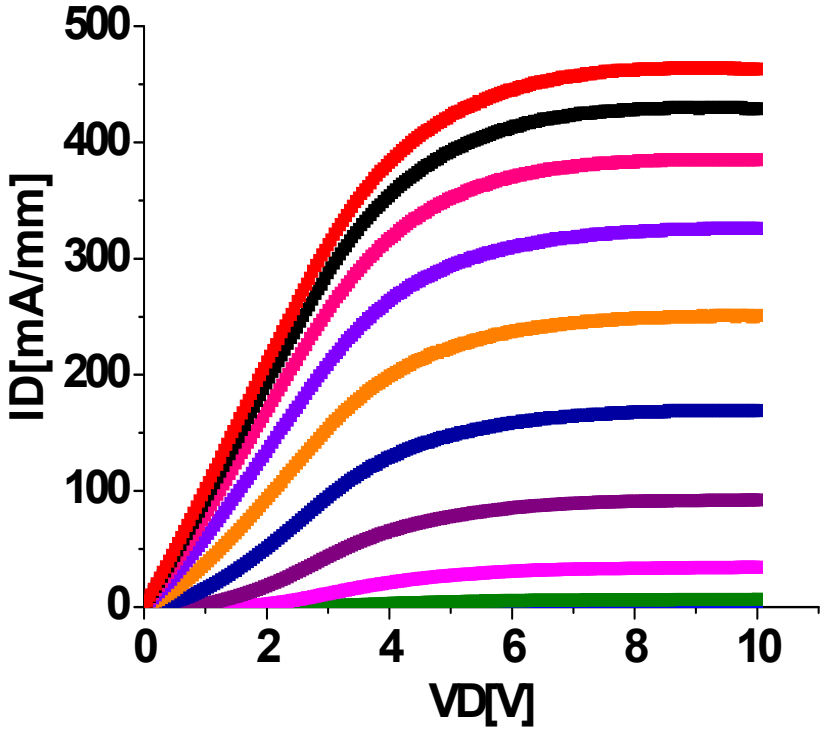


- - Undoped GaN Channel layer with p-GaN Buffer layer

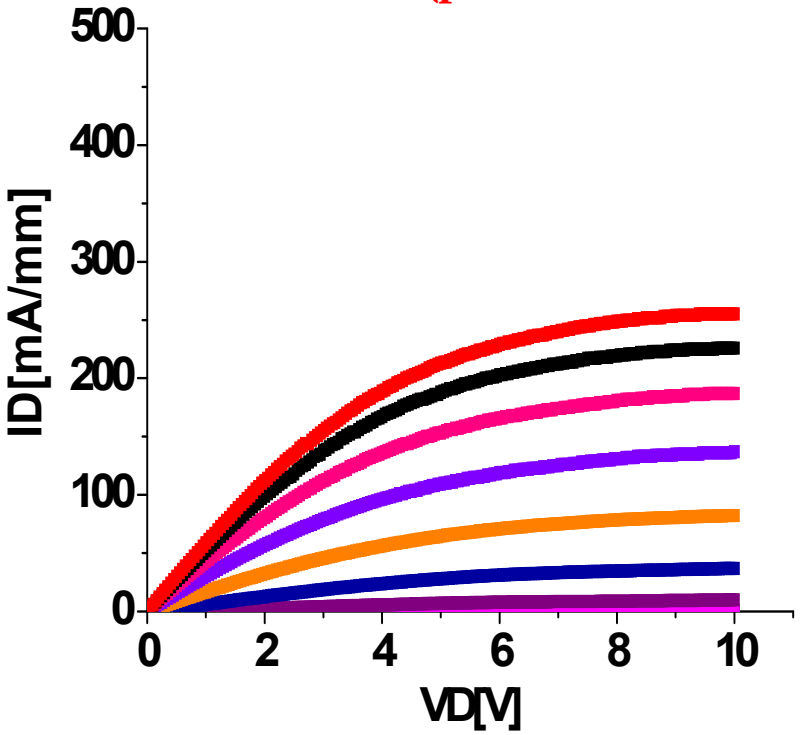
1) depleted 2DEG under the gate
   (depletion effect from p-GaN back-barrier + gate recess)
2) undepleted 2DEG under the source/drain
   (to keep 2DEG for ohmic contact)

→Investigation of the effect of thickness of the GaN-channel layer on the variation of V_t and I_{ds}

(p-GaN back barrier)

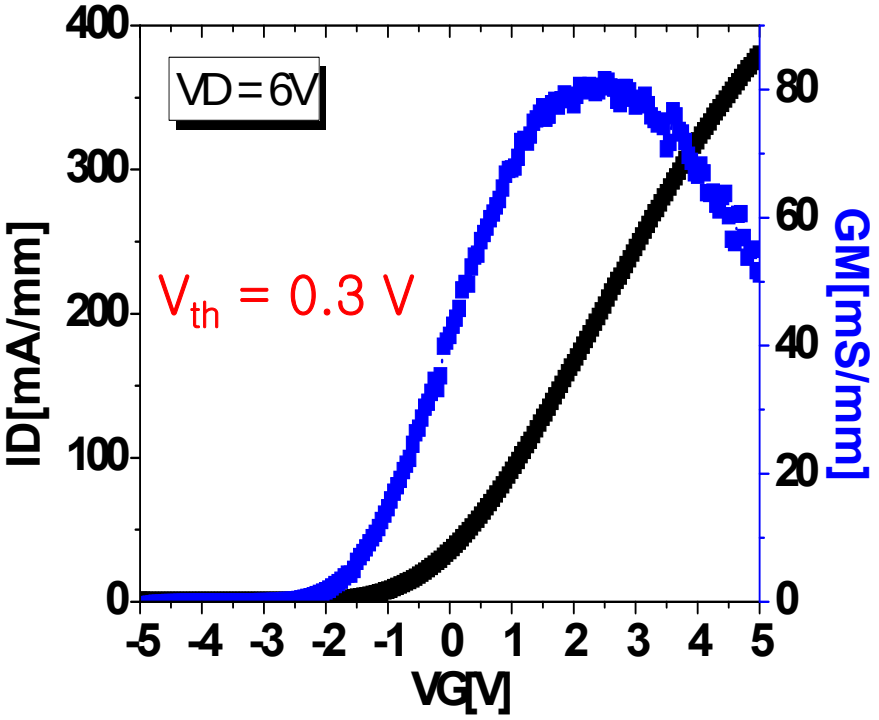


(1) Channel thickness of 400 nm

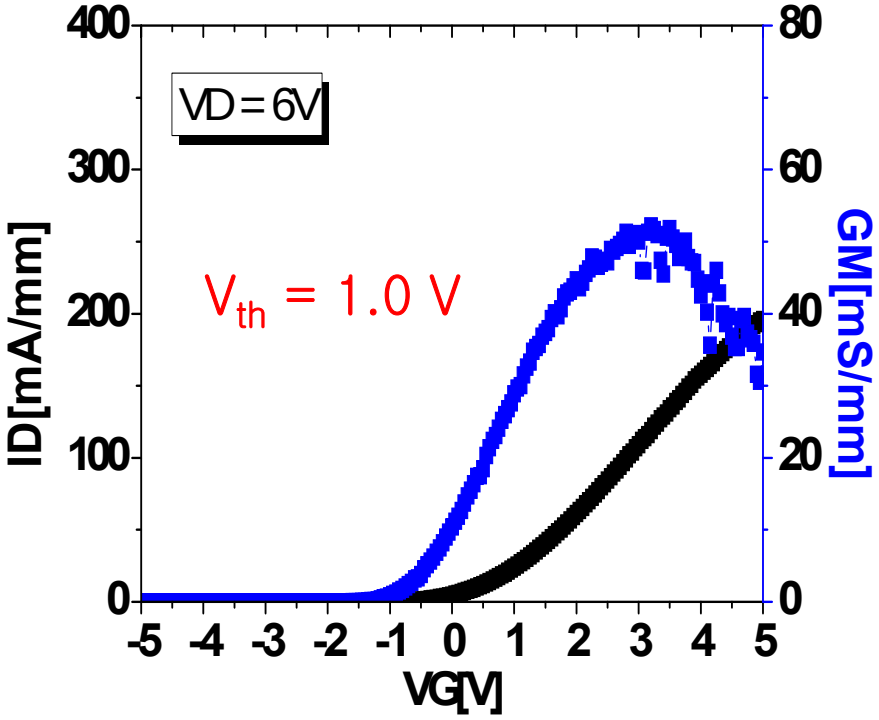


(2) Channel thickness of 250 nm

(p-GaN back barrier)

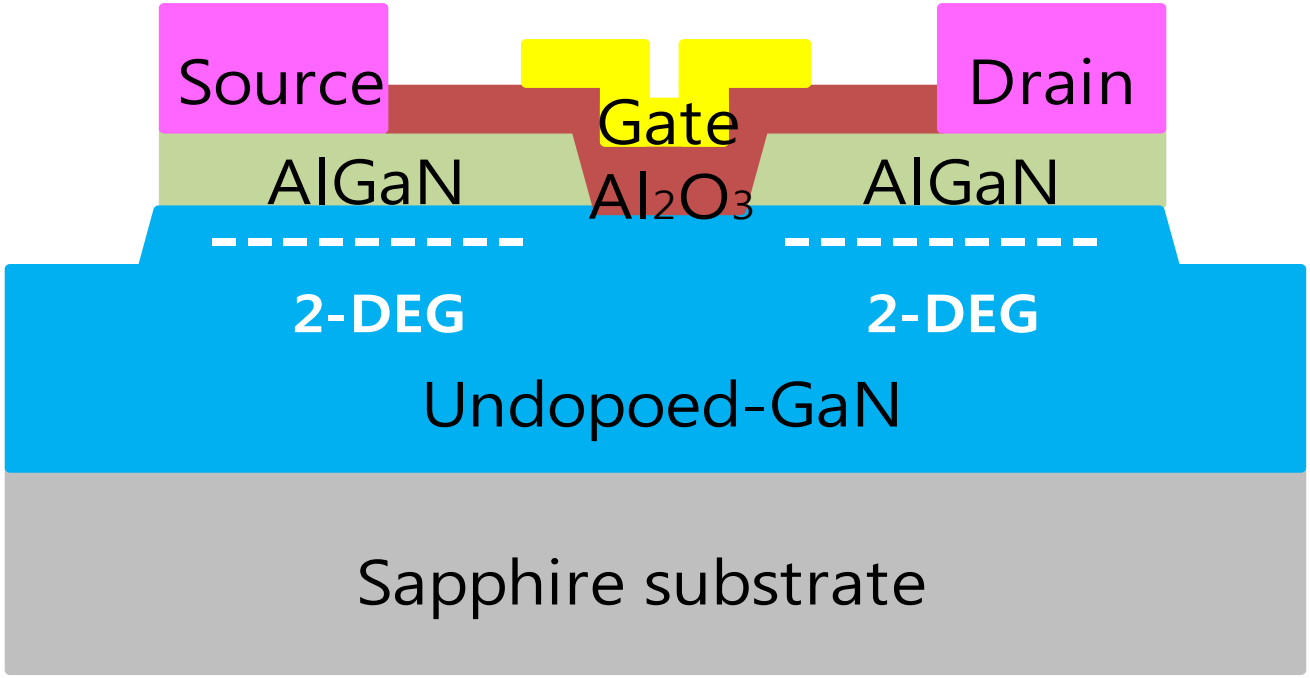


(1) Channel thickness of 400 nm



(2) Channel thickness of 250 nm

3. Normally-off GaN –MOSFET (TMAH treatment)

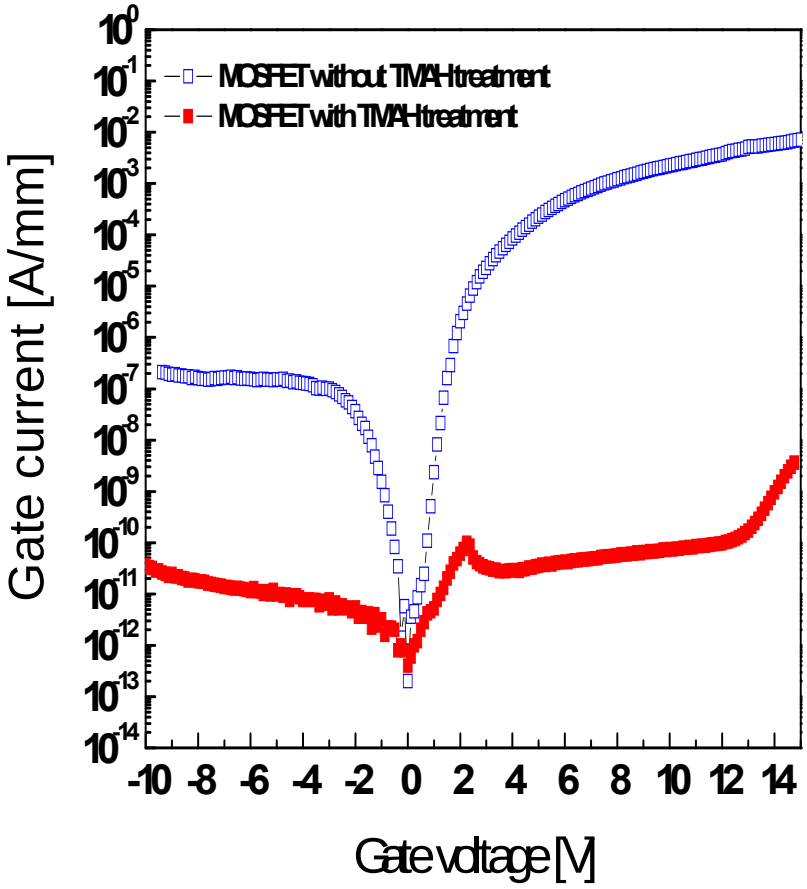


Effect of TMAH treatment

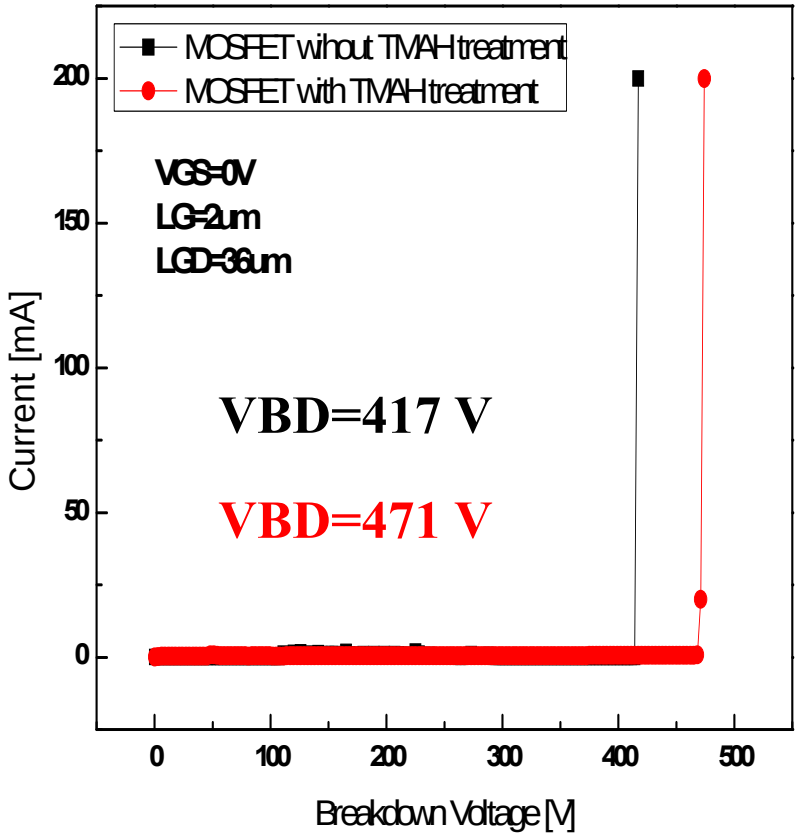
1) The effective removal of plasma damage introduced during the recess process

2) Smoothening of the recessed surface

(TMAH treatment)

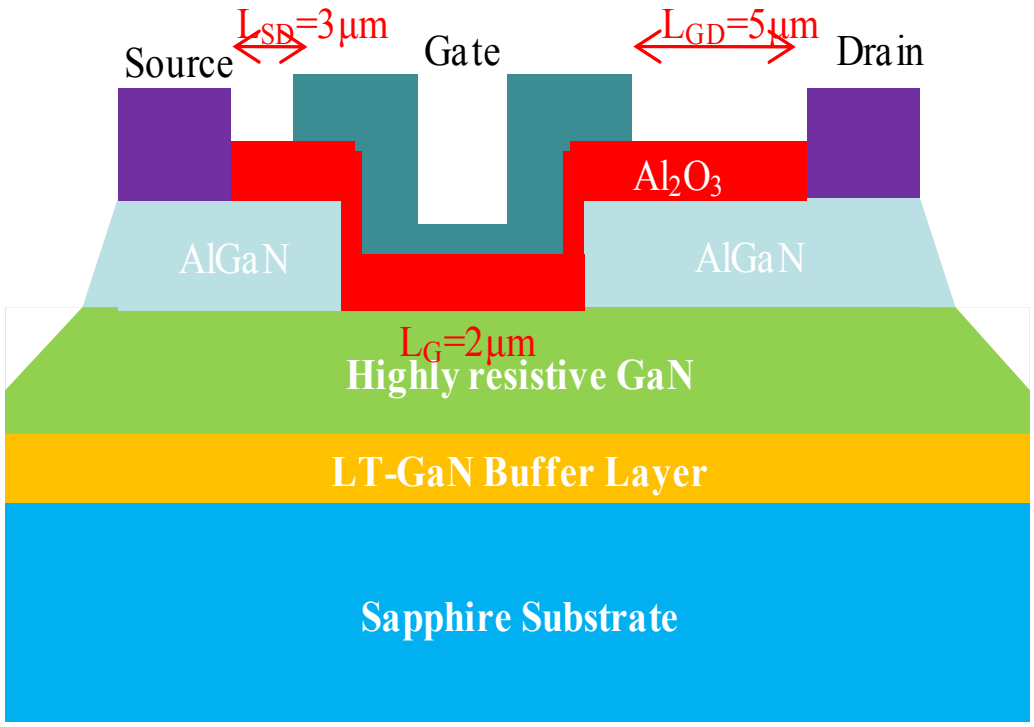


✓ Gate leakage



✓ Breakdown Characteristics

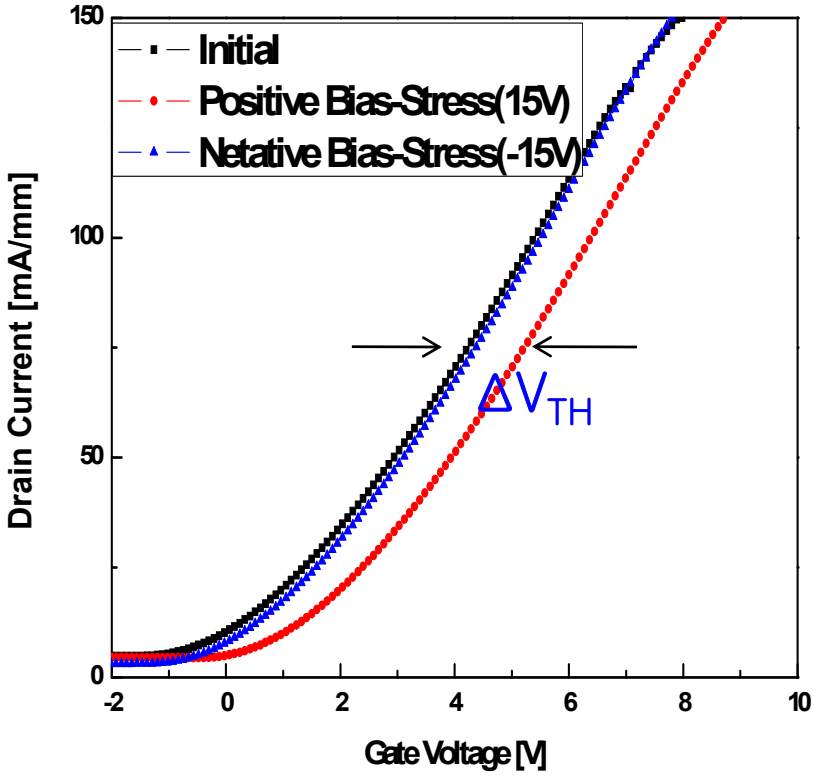
4. Normally-off GaN-MOSFET *(annealing effects)*

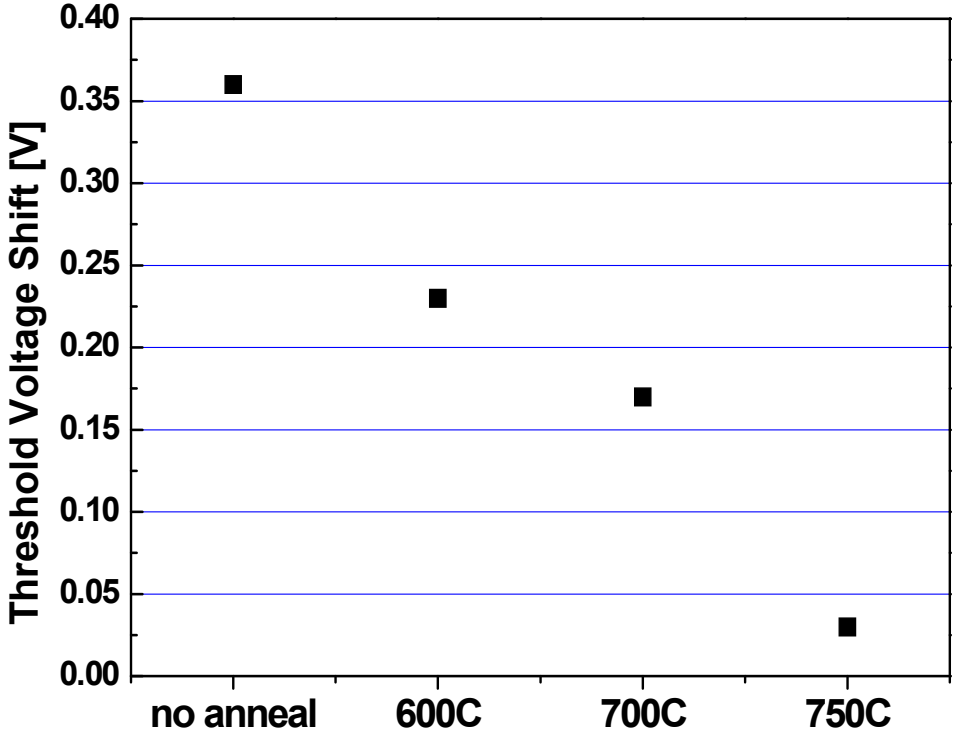


	No anneal	750C anneal
SS [mV/dec]	642	347
Dit [/cm^{2}eV]	1.29E13	5.71E12

✓ Threshold voltage shift

(annealing effects)





✓ ***Charge trapping in Al_2O_3 (ALD)***

More details will be presented in INFOS, June 2011, Grenoble.

Thank you